IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Previously Presented): A semiconductor device comprising:

a first semiconductor chip including a plurality of memory elements and a second semiconductor chip including a central processing unit (CPU) block stacked,

wherein said first semiconductor chip includes

a first electrode portion for connecting to an external electrode through wiring,

a second electrode portion having micro bumps for connecting said CPU block in said second semiconductor chip to said first electrode portion, and

a third electrode portion having micro bumps for providing a data connection from said memory block in said first semiconductor chip to said CPU block in said second semiconductor chip; and

said second semiconductor chip includes

a fourth electrode portion having micro bumps for connecting to the second electrode portion in said first semiconductor chip, and

a fifth electrode portion having micro bumps for connecting to the third electrode portion in said first semiconductor chip,

wherein the second electrode portion in said first semiconductor chip and the fourth electrode portion in said second semiconductor chip are arranged in a vicinity of a peripheral portion on each chip and the third electrode portion in said first semiconductor chip and the fifth electrode portion in said second semiconductor chip are arranged in a vicinity of a center portion on each chip.

Claim 2 (Cancelled).

Claim 3 (Cancelled).

Claim 4 (Previously Presented): The semiconductor device according to claim 1, wherein a number of micro bumps constituting said third and fifth electrode portions is at least a number corresponding to a number of bits of a memory element which is included in said first semiconductor chip and in which a readout or writing is performed in parallel.

Claim 5 (Previously Presented): The semiconductor device according to claim 1, wherein a memory element included in said first semiconductor chip is a DRAM.

Claim 6 (Previously Presented): The semiconductor device according to claim 5, wherein a number of micro bumps constituting said third and fifth electrode portions is at least equal to a bit width of each of an input and an output bus of the DRAM.

Claim 7 (Previously Presented): The semiconductor device according to claim 5, wherein a bit width of each of an input bus and an output bus of the DRAM is 128 bits, and, the number of micro bumps constituting said third and fifth electrode portions is at least 256.

Claim 8 (Previously Presented): The semiconductor device according to claim 1, wherein the first semiconductor chip includes four DRAMS.

Claim 9 (Previously Presented): The semiconductor device according to claim 8, wherein a bit width of each of an input bus and an output bus of each of the four DRAMS is 128 bits, and the number of micro bumps constituting said third and fifth electrode portions is at least 1024.

Claim 10 (Canceled).

Claim 11 (Previously Presented): A semiconductor device comprising:

a first semiconductor chip including a plurality of memory elements,

a second semiconductor chip including a central processing unit (CPU) block stacked,

a first electrode configured to connect the first semiconductor chip to an external electrode through wiring,

a second electrode having micro bumps configured to connect said CPU block in said second semiconductor chip to the first electrode,

a third electrode having micro bumps configured to provide a data connection from said memory block in said first semiconductor chip to said CPU block in said second semiconductor chip,

a fourth electrode having micro bumps configured to connect to the second electrode in said first semiconductor chip, and

a fifth electrode having micro bumps configured to connect to the third electrode in said first semiconductor chip, wherein

the second electrode in said first semiconductor chip and the fourth electrode in said second semiconductor chip are located in a vicinity of a peripheral portion on each chip, and

the third electrode in said first semiconductor chip and the fifth electrode in said second semiconductor chip are located in a vicinity of a center portion on each chip.

Claim 12 (Previously Presented): The semiconductor device according to claim 11, wherein a number of micro bumps constituting said third and fifth electrodes is at least a number of bits of a memory element which is included in said first semiconductor chip and in which a readout or writing is performed in parallel.

Claim 13 (Previously Presented): The semiconductor device according to claim 11, wherein a memory element included in said first semiconductor chip is a DRAM.

Claim 14 (Previously Presented): The semiconductor device according to claim 13, wherein a number of micro bumps constituting said third and fifth electrode portions is at least equal to a bit width of each of an input and an output bus of the DRAM.

Claim 15 (Previously Presented): The semiconductor device according to claim 13, wherein a bit width of each of an input bus and an output bus of the DRAM is 128 bits, and, the number of micro bumps constituting said third and fifth electrode portions is at least 256.

Claim 16 (Previously Presented): The semiconductor device according to claim 11, wherein the first semiconductor chip includes four DRAMS.

Claim 17 (Previously Presented): The semiconductor device according to claim 16, wherein a bit width of each of an input bus and an output bus of each of the four DRAMS is 128 bits, and the number of micro bumps constituting said third and fifth electrode portions is at least 1024.

Claim 18 (Canceled).